Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1 (currently amended). A semiconductor fabrication process, comprising:

forming an [~~interlevel dielectric (ILD)~~] ILD overlying a substrate of a semiconductor wafer wherein forming the ILD comprises:

forming a low K dielectric overlying a semiconductor substrate of the wafer, wherein a dielectric constant of the low K dielectric is less than or equal to 3.0;

forming an organic, silicon-oxide, glue layer dielectric overlying the low K dielectric; and

forming a CMP stop layer dielectric overlying the glue layer dielectric;

forming a void in the ILD;

depositing a conductive material over the wafer to fill the void; and

removing portions of the conductive material exterior to the void by polishing the wafer with a CMP process and terminating the CMP process on the CMP stop layer dielectric.

2 (original). The method of claim 1, wherein forming the glue layer dielectric and the CMP stop layer dielectric comprises:

forming a plasma within a CVD reactor chamber using a specified set of precursors including a carbon bearing precursor and maintaining the plasma during formation of the glue layer dielectric; and

following formation of the glue layer dielectric, reducing a flow rate of the carbon bearing precursor while continuing to maintain the plasma to form the CMP stop layer dielectric wherein the CMP stop layer dielectric is substantially free of carbon.

3 (original). The method of claim 2, wherein the specified set of precursors includes an oxygen bearing precursor and a second precursor selected from tetramethylsilane (4MS) and trimethylsilane (3MS).

4 (original). The method of claim 3, wherein a ratio of the oxygen precursor flow rate to the second precursor flow rate is less than 1:2 while forming the glue layer dielectric and further wherein the ratio exceeds 2:1 while forming the CMP stop layer dielectric.

5 (original). The method of claim 4, wherein the reactor chamber temperature and pressure are maintained at constant during the formation of the glue layer dielectric and the CMP stop layer dielectric.

6 (original). The method of claim 2, wherein forming the low K dielectric comprises spinning on a low K material.

7 (original). The method of claim 2, wherein forming the low K dielectric comprises depositing an OctaMethylCycloTetra Siloxane (OMCTS) material.

8 (currently amended). A method of forming an [~~interlevel dielectric (ILD)~~] ILD overlying a substrate of a semiconductor wafer, comprising:

forming a first dielectric having a dielectric constant less than or equal to 3.0 overlying the substrate;

depositing, with a chemical vapor deposition process, second and third dielectrics overlying the first dielectric, wherein forming the second and third dielectrics comprises forming a plasma from an oxygen bearing precursor and an organic precursor, maintaining the flow rates of the precursors at first flow rates while forming the second dielectric, and thereafter, reducing the relative flow rate of the organic precursor while maintaining the plasma to form the third dielectric.

9 (original). The method of claim 8, wherein forming the first dielectric comprises spinning on a silsesquioxane-based film.

10 (original). The method of claim 8, wherein forming the first dielectric comprises depositing an OctaMethylCycloTetra Siloxane (OMCTS)-based film.

11 (original). The method of claim 8, wherein the second dielectric comprises an organic silicon-oxide, and further wherein the third dielectric comprises substantially carbon-free silicon-oxide.

12 (original). The method of claim 8, wherein the organic precursor comprises an precursor selected from 3MS and 4MS.

13 (original). The method of claim 12, wherein a ratio of the oxygen precursor flow rate to the organic precursor flow rate is less than 1:2 while forming the second dielectric and further wherein the ratio exceeds 2:1 while forming the third dielectric.

14 (original). The method of claim 13, wherein a temperature and pressure of a reactor chamber of the CVD process remain constant during formation of the second and third dielectrics and further wherein an radio frequency power of the reactor chamber is uninterrupted during formation of the second and third dielectrics.

15 (original). A semiconductor fabrication process, comprising:

forming a first dielectric having a dielectric constant of less than or equal to 3.0 over a semiconductor substrate;

forming, in a chemical vapor deposition (CVD) reactor chamber using a continuously maintained plasma derived from an oxygen precursor and an organic precursor, a second dielectric overlying the first dielectric and a third dielectric overlying the second dielectric, wherein the second dielectric comprises an organic silicon-oxide and the third dielectric comprises a substantially carbon free silicon-oxide.

16 (original). The method of claim 15, wherein forming the first dielectric comprises spin depositing a silsesquioxane-based material overlying the substrate.

17 (original). The method of claim 15, wherein forming the first dielectric comprises depositing an OctaMethylCycloTetra Siloxane (OMCTS)-based film overlying the substrate.

18 (original). The method of claim 15, wherein the organic precursor comprises 3MS or 4MS.

19 (original). The method of claim 18, wherein the flow rate of the organic precursor exceeds the flow rate of the oxygen precursor while forming the second dielectric and the organic precursor flow rate is less than the oxygen precursor flow rate during while forming the third dielectric.

20 (original). The method of claim 19, wherein the CVD reactor temperature and pressure are maintained at constant values during formation of the second and third dielectrics.

21 (new). The method of claim 1, wherein the ILD comprises an intralevel dielectric.

22 (new). The method of claim 1, wherein the ILD comprises an interlevel dielectric.

23 (new). The method of claim 1, wherein terminating on the CMP stop layer includes removing a portion of the CMP stop layer.

24 (new). The method of claim 8, wherein ILD comprises an intralevel dielectric.

25 (new). The method of claim 8, wherein ILD comprises an interlevel dielectric.